21992 Wax

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Packet Radio Temporary Note #92

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MICROPROCESSOR COMPONENTS

1.0 INTRODUCTION

The purpose of this investigation was to characterize the technology of microprocessor components, memories and structures. The study is heavily weighted in favor of components that are available now. The many designs that are being planned or that are on-going at the various semiconductor houses are not considered in this evaluation. It is felt that there is not enough assurance that these devices will be available for equipment delivery in 1974.

2.0

Refer to Table 1 for a list of the microprocessor sets available. Also included are lists of random access memories and programmable read only memories.

A listing of the several factors considered in evaluating the various component sets is included in the following tables:

Table 2 - MOS Random Access Memories
Table 3 - MOS PROMS
Table 4 - CPU Parameters Used in Evaluation

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Table 5 - RAM Parameters Used in Evaluation
Table 6 - Comparison of Microprocessor Sets

3.0 CONCLUSIONS

Based in the investigation, the following selections have been made:

A) The National General Purpose Controller/Processor appears most promising for the Packet Radio repeater requirements.

B) Complimentary MOS (C-MOS) for Random Access Memories.

C) Programmable (electrically erasable) Read Only Memories will be used.

Table 5 - RAM Parameters Used in Evaluation
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TABLE 1

COMPANIES WITH MICROPROCESSOR SETS

1. INTEL - 4 BIT - 4004, 8 BIT - 8008, BOTH ARE SINGLE CHIP CPU'S.
2. NATIONAL SEMICONDUCTOR - MULTICHIP CPU, CAN CHOOSE WORD WIDTH.
3. ROCKWELL-MICROELECTRONICS - 4 BIT SINGLE CHIP CPU.
4. FAIRCHILD - PPS 25 - DECIMAL ORIENTED SET.

COMPANIES WITH PLANS FOR MICROPROCESSOR SETS

1. INTEL - 8 BIT N-CHANNEL CPU - 8080 - DEC. 73.
2. MOTOROLA - 8 BIT N-CHANNEL CPU - FIRST QUARTER 74.
3. ROCKWELL-MICROELECTRONICS - 8 BIT CPU.
4. WESTERN DIGITAL CORP. - 8 BIT N-CHANNEL CPU - BEFORE 74.
5. SIGNETICS - NO INFORMATION.
6. HUGHES AIRCRAFT CO. - NO INFORMATION.
7. AMI - 16 BIT GENERAL PURPOSE SET.

TABLE 2

MOS RAM'S

	INTEL				MOSTEK	NATIONAL		EA	RCA AMS (256 BIT)	
	1103-1	2102	2102-1	2105-1	4006-6	4260	5260	1502	6002	CD4061
imum Power Dissipation (MW)	475	300	300	500	575	575	575	165	275	80
ical Power Dissipation (MW)	375	150	150	325	400	400	400	100	180	5
ndby. Power (MW)	75	150	150	65	50 50	100	100	30	2	25µw
ess Time (N. Sec)	150	700	350	80	400	450	375	150	150	280
le Times: Read (N. Sec)	300	1000	500	180	400	600	500	290	250	400
Write (N. Sec)	340	1000	500	180	650	750	625	450	250	500
e of Input	Mos[1]	TTL[2]	TTL[2]	Mos-TTL[3]	TTL[2]	Mos-TTL[3]	Mos-TTL[3]	Mos-TTL[3]	Mos [1]	TTL[2]
e of Output	Current Sense	TTL	TTL	Current Sense	Current Sense	TTL	TTL	TTL	Current Sense	TTL
resh Interval/No. Of Refresh Cycles	2M Sec 32 Cycles	Static	Static	10µ Sec 1 Cycle	2m Sec 32 Cycles	1m Sec 32 Cycles	2m Sec 32 Cycles	2m Sec 1 Cycle	2m Sec 32 Cycles	Static
rating Temperature	0°C TO 70°C	0°C TO 70° C	0°C TO 70°C	0°C TO 70°C	0°C TO 70°C	-55°C TO 125°C	-25°C TO 70°C	0°C TO 70°C	0°C TO 70°C	-55°C TO 125°C
er Supplies (Volts)	+19, +22	+5	+5	+12, -5	+5, -12	+5, -12	+5, -12	± 12	+7, +20 +22.5	Variable +3-+15
Of Pins	18	18	18	18	16	16	16	18	22	16
ces, 1-24 Quantities	$13.50	$24.00	$44.50	$60.00	$16.75	$47.80	$18.00	$41.20	$25.00	$12.00
Of Level Shifters And se Amps-1024x8 Bit	29	0	0	10	8	2	2	2	29	0
e of Mos	P	N	N	N	P	P	P	N	P	Both

1. Mos - 15-20V Voltages Swings Are Needed.
2. TTL - 5V Logic Levels
3. Mos-TTL-Part Of The Inputs Require Mos Voltages And Part Can Be Driven By TTL Levels.

TABLE 3

MOS ELECTRICALLY PROGRAMMABLE AND ERASABLE ROM'S

		Intel 1702A	National MM4203
1.	Power Dissipation	700 mw	700 mw
2.	Cycle Time	700 n sec.	700 nsec.
3.	Chip Enable Logic	Single Line	3 Bit Control
4.	TTL Compatible	Yes	Yes
5.	Power Supplies	+5, -9	+5, -12
6.	No. of Pins	24	24
7.	Operating Temp.	0°C to 70°C	-55°C to 85°C
8.	Required Clocks	None	None

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TABLE 4

CPU PARAMETERS USED IN EVALUATION: REFER TO TABLE 6

1. Power Requirements - Includes CPU, supporting circuitry, and 1 I/O port. Does not include any memory.
2. Program Execution Efficiency - Predicted operating time for a particular benchmark program.
3. Supporting Circuitry Required - The number of IC's required to make the CPU a workable system. Does not include memory or TTY interface.
4. Program Storage Efficiency - The number of memory locations necessary to store a benchmark program.
5. Power Supplies
   a. Number required
   b. Voltages required are the voltages of common usage?
6. I/O Interfacing
   a. Ease of design - what's available to aid hardware design?
   b. Number of input and output ports.
   c. Software - what's available under software control?
7. P.C.B. partitioning ease - breaking up components on 2 or 3 boards, how many pin-outs are necessary?
8. Clock requirements
   a. Frequency - is it easy to derive?
   b. Number of phases
   c. TTL or MOS level
9. Allowable voltage fluctuations or ripple

TABLE 4 (Cont'd)

10. Cost
    a. CPU chip(s)
    b. Supporting circuitry
    c. P.C. boards
    d. Prototype kit
11. Memory addressing
    a. Direct
    b. Indirect
    c. Indexed
    d. Literal
12. Instruction set utility
    a. Number of instructions
    b. Number of different instruction types
    c. Unusual instructions
13. Number of registers
    a. Accumulato~
    b. Index
    c. Scratch pad
14. Stack capabilities
    a. Size of stack
    b. Is it accessible through software?
15. Largest memory capacity addressable
16. Capability for customer microprogramming

TABLE 5

RANDOM ACCESS MEMORY PARAMETERS USED IN EVALUATION: REFER TO TABLE 6

1. Cost per bit - interface and control circuitry included. (Refresh circuitry included if necessary).
   a. 1024 word x 8 bit system
   b. 1024 word x 16 bit system
2. Power dissipation per bit - interface and control circuitry. (Refresh circuitry included if necessary).
3. Cycle Times
   a. Access - time from chip select until data available.
   b. Read - access time plus deselect time.
   c. Write/refresh
4. Refresh requirements
   a. Number of address changes required for complete memory refresh.
   b. Minimum time between refreshed.
5. TTL compatibility
6. Operating temperature - if not specified over the military range, will the memory function at high temperatures.
7. Power supplies
   a. Number required
   b. Voltages required - are the voltages of common usage?
8. Availability
   a. Can the part be had in large quantities?
   b. Second sourced
   c. State of the art - is it the current design?
9. Packaging Efficiency - Using 16,192 bits as a standard, how many IC's are necessary to produce a memory system with interface, control, and refresh circuitry included.

	8008-1
1. Power Requirements (Watts)	With TTL - 7W With CMOS - 1W
2. Program Execution Efficiency	
3. Supporting Circuitry Required	37 IC's
4. Program Storage Efficiency	124 Words x 8 Bits
5. Power Supplies	+5V, -9V
6. I/O Interfacing	8 possible I/O Ports No Input Lines for communicating with CPU except Control Panel Interrupt
7. P.C.B. Partitioning	An 8 Bit Bidirectional bus is used for Data I/O and Addressing. This allows for fewer Pin Outs from board.
8. Clock Requirements	TTL Level Clocks 2 Phase
9. Allowable Voltage Fluctuations	+5%
10. Cost	CPU Chip - $180 SIM 8-01 - $900 INTELLEC - 8 $3650
11. Memory Addressing	Indexed only
12. Instruction Set Utility	48 Instructions
13. Number of Registers	1 8-Bit Accumulator 6 General Registers 2 of the 6 can be used for Indexing
14. Stack Capabilities	7 14-Bit Registers for Program Counter Storage only
15. Largest Memory Addressable	16K word x 8 Bit
16. Capability for Microprogramming	None

TABLE 6

COMPARISON OF MICROPROCESSOR SETS

IMP-16	IMP-8
With TTL - 14W With CMOS - 3W	With TTL - 8W With CMOS - 2W
40 IC's	34 IC's
49 Words x 16-Bits	
+5V, -12V	+5V, -12V
6 General Purpose Flags 4 General Purpose Jump condition inputs 1 General Interrupt Input	Same as IMP-16
16-Bit Bidirectional bus is used for I/O and Addressing. The wider word and greater number od CPU lines makes for more Pin Outs	8-Bit Bidirectional bus is used for I/O and Addressing
-12V to +5V Swing 4 Phase	-12V to +5V 4 Phase
±5%	±5%
CPU Chips - $430 IMP - 16C - $950 IMP - 16P - $3850	CPU Chips - $270 IMP - 8C - $800 IMP - 8P - $3750
Direct, Indirect, Indexed, Literal Relative Type	Direct, Indirect, Indexed, Literal Paged Type
43 Instructions Software Control of Stack and External Flags. External Jump Condition Inputs	38 Instructions Software Control of Stack And External Flags. External Jump Condition Inputs
4 16-Bit Accumulators	4 16-Bit Accumulators
16 16-Bit Registers Accessable through Software	16 8-Bit Registers Accessable through Software
65K word x 16-Bit	65K word x 8-Bit
Instruction Sets can be developed	Same as IMP-16